QPro Virtex-II 1.5V Platform FPGAs

DS122 (v3.0) April 7, 2014

Product Specification

Summary of QPro™ Virtex™-II Features

- Industry's first military-grade platform FPGA solution
- Certified to MIL-PRF-38535 (Qualified Manufacturer Listing)
- 100% factory tested
- Guaranteed over the full military temperature range (–55°C to +125°C) or industrial temperature range (–40°C to +100°C)
- Ceramic and plastic wire-bond and flip-chip grid array packages
- IP-immersion architecture
  - Densities from 1M to 6M system gates
  - 300+ MHz internal clock speed (Advance Data)
  - 622+ Mb/s I/O (Advance Data)
- SelectRAM™ Memory Hierarchy
  - 2.5 Mb of dual-port RAM in 18 Kbit block SelectRAM resources
  - Up to 1 Mb of distributed SelectRAM resources
- High-performance interfaces to external memory
  - DRAM interfaces
    - SDR/DDR SDRAM
    - Network FCRAM
    - Reduced Latency DRAM
  - SRAM interfaces
    - SDR/DDR SRAM
    - QDR SRAM
  - CAM interfaces
- Arithmetic functions
  - Dedicated 18-bit x 18-bit multiplier blocks
  - Fast look-ahead carry logic chains
- Flexible logic resources
- Up to 67,584 internal registers/latches with Clock Enable
- Up to 67,584 look-up tables (LUTs) or cascadable 16-bit shift registers
- Wide multiplexers and wide-input function support
- Horizontal cascade chain and sum-of-products support
- Internal 3-state busing
- High-performance clock management circuitry
  - Up to 12 DCM (Digital Clock Manager) modules
    - Precise clock de-skew
    - Flexible frequency synthesis
    - High-resolution phase shifting
  - 16 global clock multiplexer buffers
- Active interconnect technology
  - Fourth-generation segmented routing structure
  - Predictable, fast routing delay, independent of fanout
- SelectIO™-Ultra Technology
  - Up to 824 user I/Os
  - 19 single-ended and six differential standards
  - Programmable sink current (2 mA to 24 mA) per I/O
  - Digitally Controlled Impedance (DCI) I/O: on-chip termination resistors for single-ended I/O standards
  - PCI compliant (32/33 MHz) at 3.3V
  - Differential signaling
  - 622 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
  - Bus LVDS I/O
  - Lightning Data Transport (LDT) I/O with current driver buffers
  - Low-Voltage Positive Emitter-Coupled Logic (LVPECL) I/O
  - Built-in DDR input and output registers
  - Proprietary high-performance SelectLink Technology
    - High-bandwidth data path
    - Double Data Rate (DDR) link
    - Web-based HDL generation methodology
- Supported by Xilinx Foundation Series™ and Alliance Series™ Development Systems
  - Integrated VHDL and Verilog design flows
  - Compilation of 10M system gates designs
  - Internet Team Design (ITD) tool

Virtex-II Ordering Information

Notes:

1. -4 and- 5 are the only supported speed grades.