



TGA2512

X Band Low Noise Amplifier

Product Overview

The Qorvo TGA2512 is a wideband LNA with AGC amplifier for EW, ECM, and RADAR receiver or driver amplifier applications. Offering high gain 27 dB typical from 5-15 GHz, the TGA2512 provides excellent noise performance with typical midband NF 1.4 dB, while the balanced topology offers good return loss typically 15 dB.

The TGA2512 is designed for maximum ease of use. The large input FETs can handle up to 21 dBm input power reliably, while the build-in gain control provides 15 dB of typical gain control range. The part is also assembled in self-biased mode, using a single +5 V supply connection from either side of the chip, or in gate biased mode, allowing the user to control the current for a particular applications.

In self-biased mode the TGA2512 offers 6 dBm typical P1 dB, while in gate-biased mode the typical P1 dB is over 13 dBm. The small size of 2.46 mm² allows ease of compaction into Multi-Chip-Modules (MCMs).

The TGA2512 is 100% DC and RF tested on-wafer to ensure performance compliance.

Key Features

- Typical Frequency Range: 5-15 GHz
- 1.4 dB Nominal Noise Figure
- 27 dB Nominal Gain
- Bias: 5 V, 160 mA Gate Bias, 5 V, 90 mA Self Bias
- 0.15 μ m 3 MI pHEMT Technology
- Chip Dimensions 2.05 x 1.20 x 0.10 mm (0.081 x 0.047 x 0.004 in)

Applications

- X-Band Radar
- EW, ECM
- Point-to-Point Radio

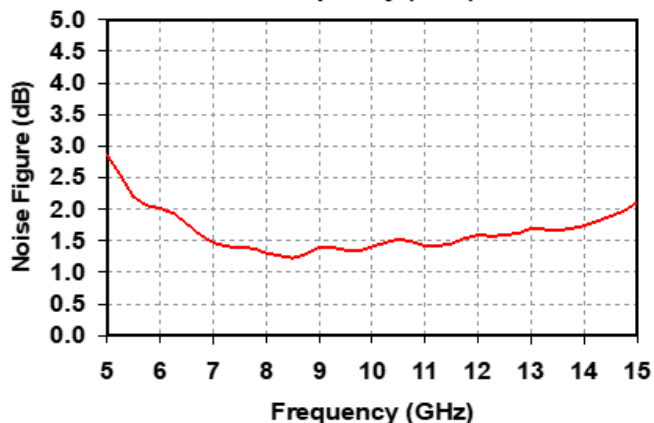
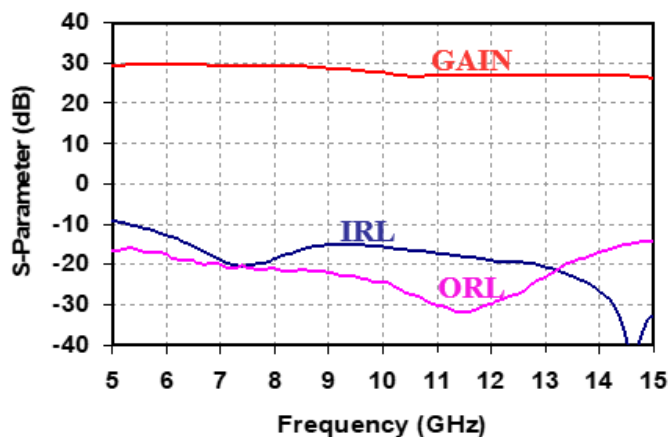
Ordering Information

Part No.	Package Style
TGA2512	X Band Low Noise Amplifier



Measured Data

Bias Conditions: Gate Bias Vd = 5 V, Id = 160 mA



Maximum Ratings 1/

Symbol	Parameter	Value	Notes
V _d	Drain Voltage	Gate Bias: $[3.5 + (0.0125)(I_d)]$ V Self Bias: $[3.5 + (0.0360)(I_d)]$ V	<u>2/</u> <u>3/</u>
V _g	Gate Voltage Range	-1 TO +0.5 V	
I _d	Drain Current (gate biased)	240 mA	<u>2/</u> <u>4/</u>
I _g	Gate Current	7.04 mA	<u>4/</u>
P _{IN}	Input Continuous Wave Power	21 dBm	
P _D	Power Dissipation	1.56 W	<u>2/</u> <u>5/</u>
T _{CH}	Operating Channel Temperature	200 °C	<u>6/</u> <u>7/</u>
	Mounting Temperature (30 Seconds)	320 °C	
T _{STG}	Storage Temperature	-65 to 150 °C	

- 1/. These ratings represent the maximum operable values for this device.
- 2/. Combinations of supply voltage, supply current, input power, and output power shall not exceed PD.
- 3/. Unit for I_d is mA
- 4/. Total current for the entire MMIC.
- 5/. When operated at this bias condition with a base plate temperature of 70 °C, the median life is 3.4 E5.
- 6/. Junction operating temperature will directly affect the device median time to failure (T_m). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
- 7/. These ratings apply to each individual FET.

DC Probe Tests (Ta = 25 °C, Nominal)

Symbol	Parameter	Min.	Typ.	Max.	Units
V _{BVGS, Q1}	Breakdown Voltage Gate-Source	-30		-5	V
V _{P, Q1,2,4,5,6}	Pinch-Off Voltage	-0.7		-0.1	V

Note: Q1, Q4, Q5 are 400 um FETs. Q2, Q6 are 300 um FETs.

Electrical Characteristics (Ta = 25 °C, Nominal)

Parameter	Gate Bias	Self Bias	Units
Frequency Range	5 - 15	5 - 15	GHz
Drain Voltage, V _d	5.0	5.0	V
Drain Current, I _d	160	90	mA
Gate Voltage, V _g	-0.1	-	V
Small Signal Gain, S ₂₁	27	24	dB
Input Return Loss, S ₁₁	15	15	dB
Output Return Loss, S ₂₂	20	20	dB
Noise Figure, NF	1.4	1.4	dB
Output Power @ 1 dB Gain Compression, P _{1 dB}	13	6	dBm
OIP ₃	24	16	dBm

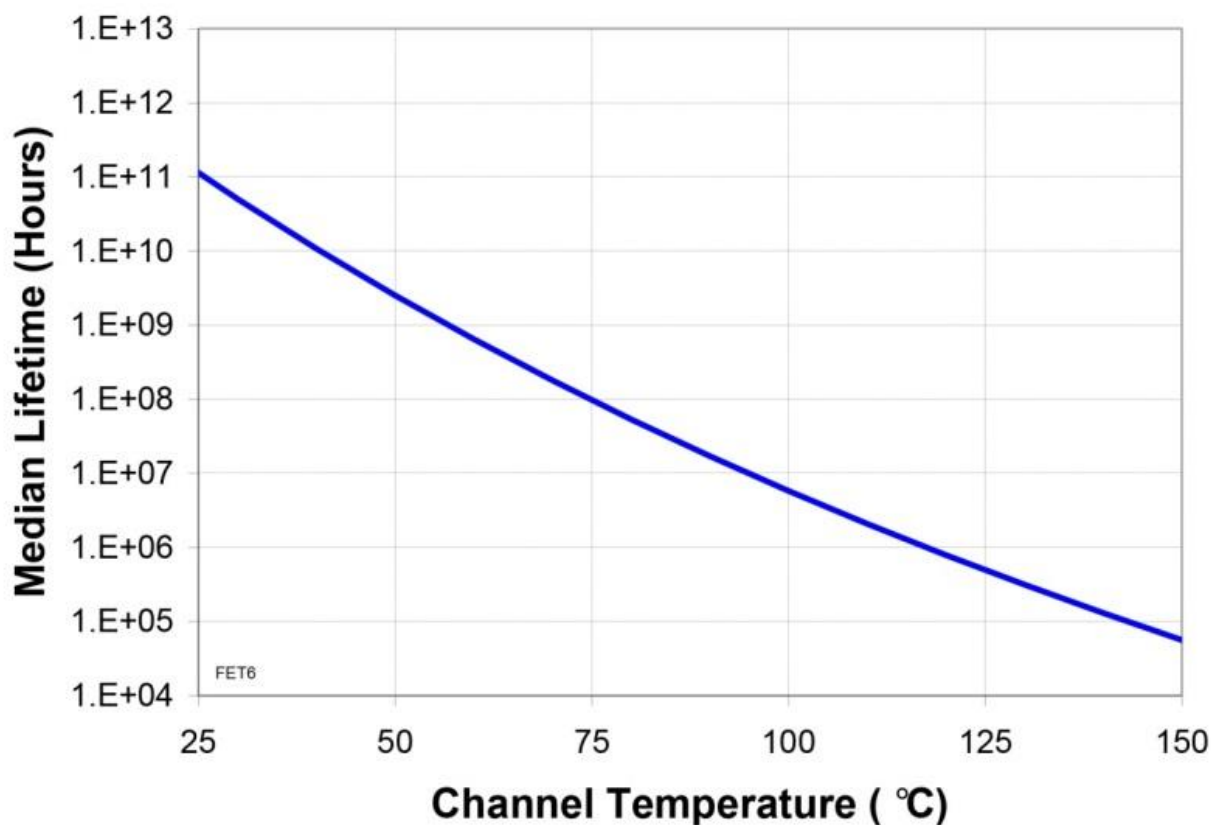
Note: Test data de-embedded to reference lines at the package RF I/O leads

Thermal Information

Parameter	Test Conditions	T_{ch} (°C)	θ_{jc} (°C/W)	T_m (Hrs)
θ_{jc} Thermal Resistance (channel to Case)	$V_d = 5\text{ V}$ $I_d = 160\text{ mA}$ Gate Bias $P_{diss} = 0.80\text{ W}$	100	37.6	5.8E+6
θ_{jc} Thermal Resistance (channel to Case)	$V_d = 5\text{ V}$ $I_d = 90\text{ mA}$ Self Bias $P_{diss} = 0.45\text{ W}$	82.7	28.2	4.1E+7

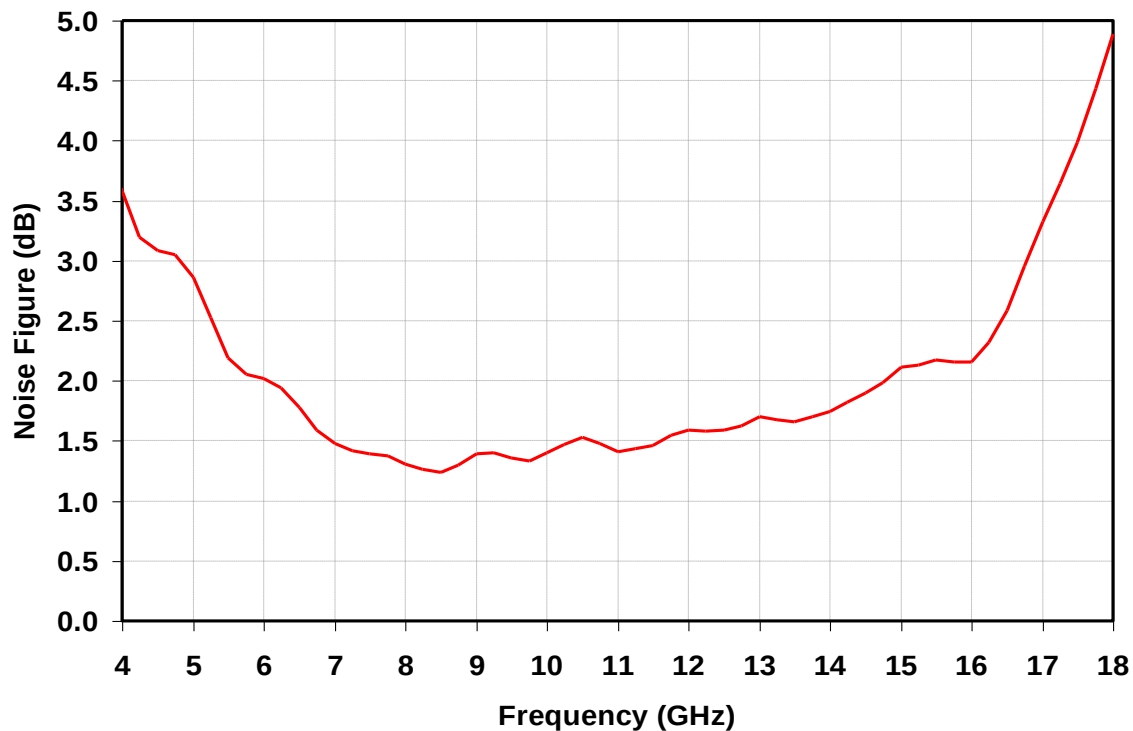
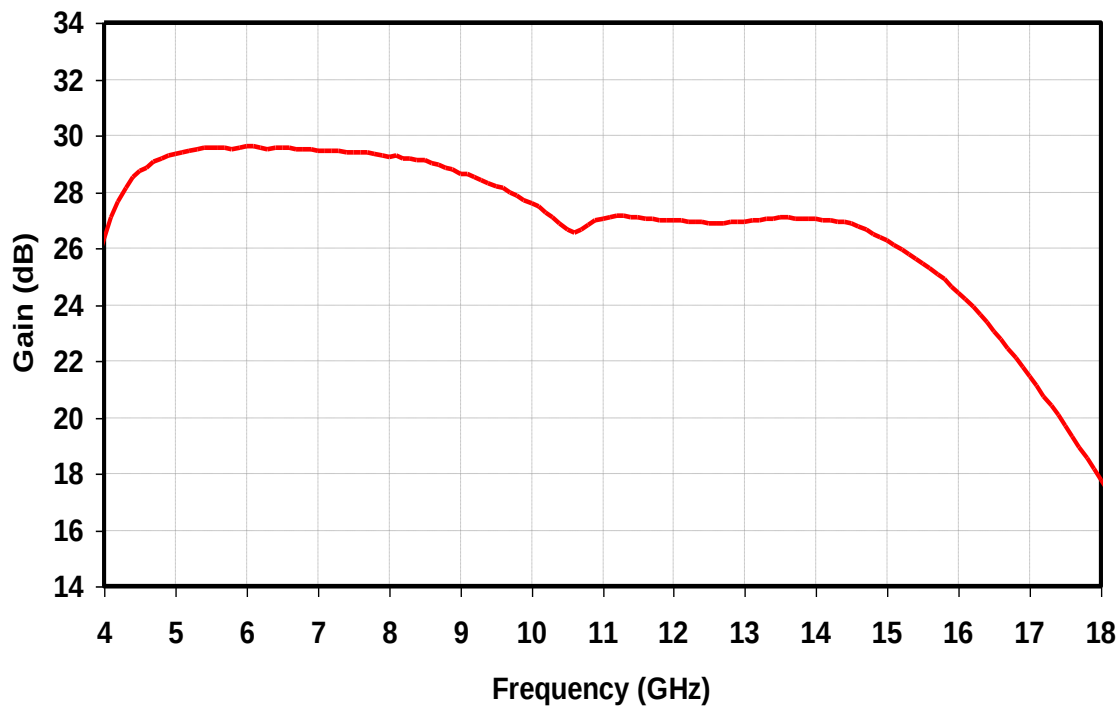
Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70 °C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

Median Lifetime (T_m) vs. Channel Temperature



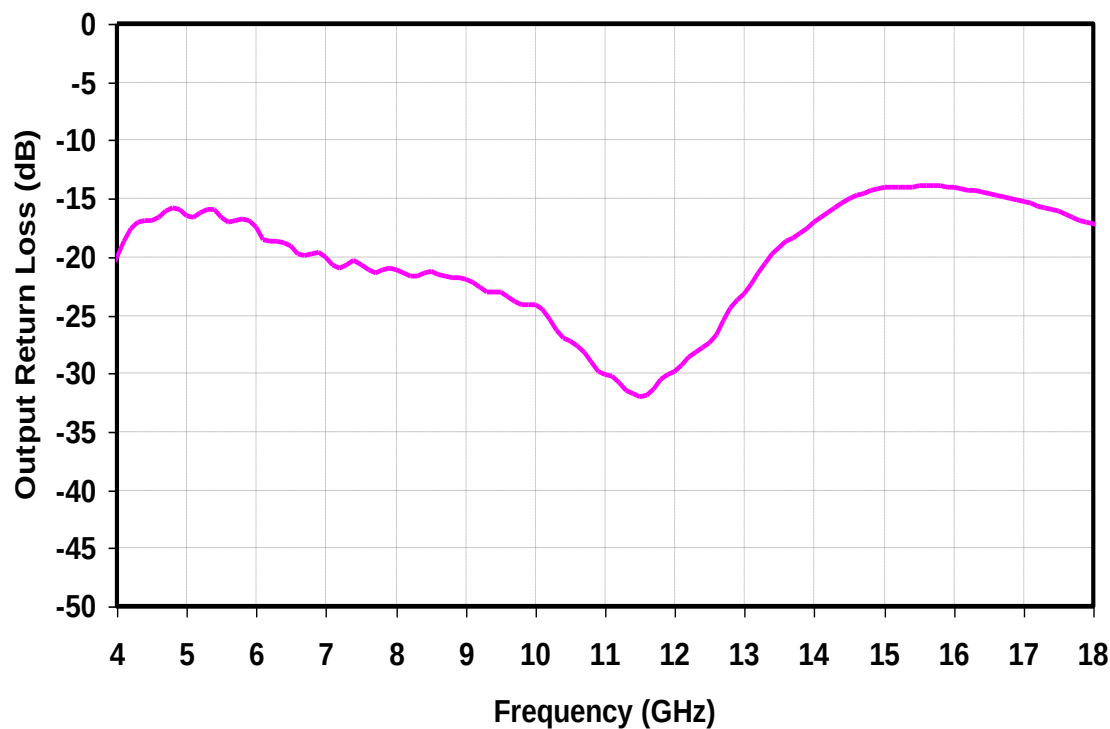
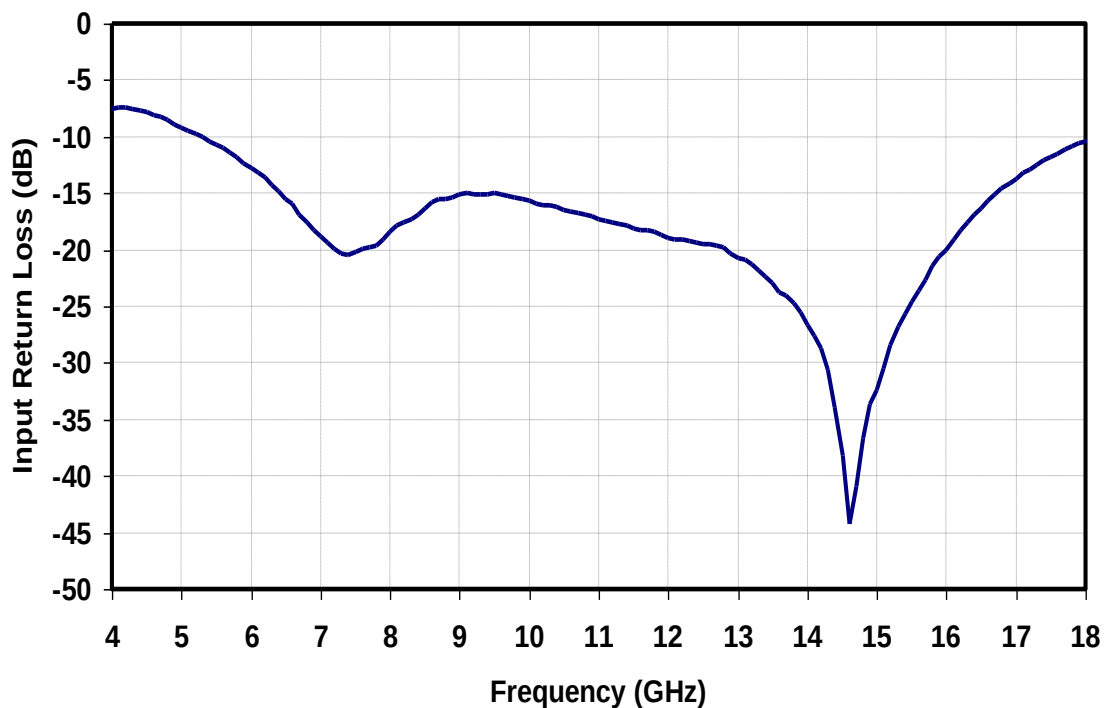
Performance Plots

Bias Conditions: Gate Bias $V_d = 5\text{ V}$, $I_d = 160\text{ mA}$, $25\text{ }^{\circ}\text{C}$



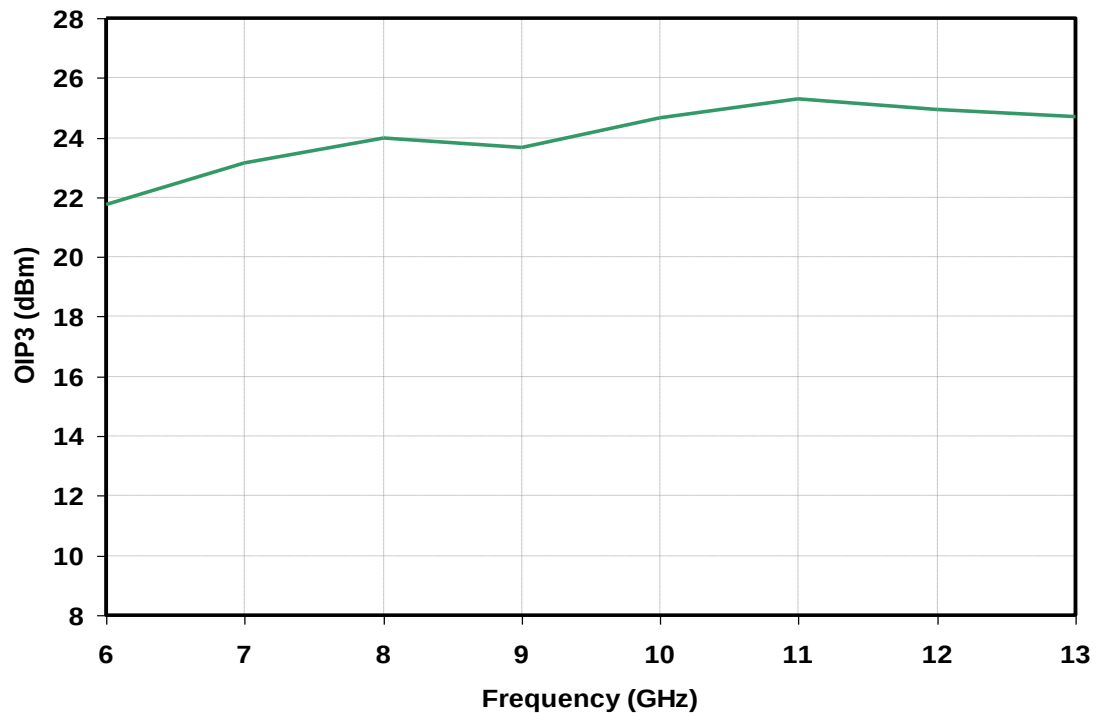
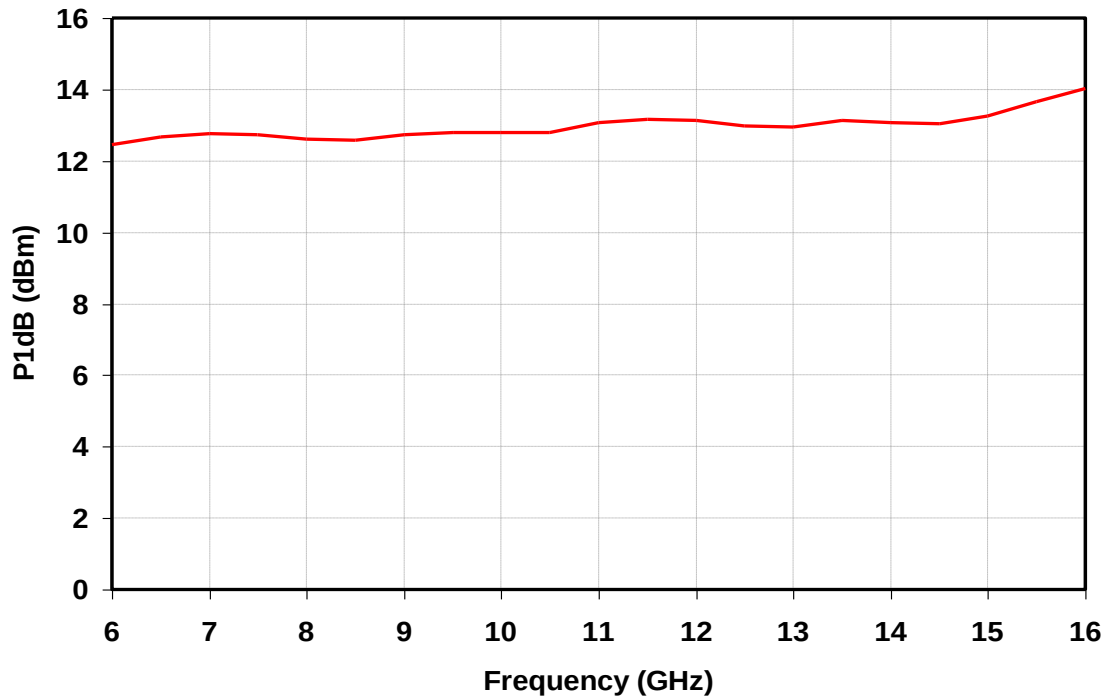
Performance Plots

Bias Conditions: Gate Bias $V_d = 5$ V, $I_d = 160$ mA, 25°C



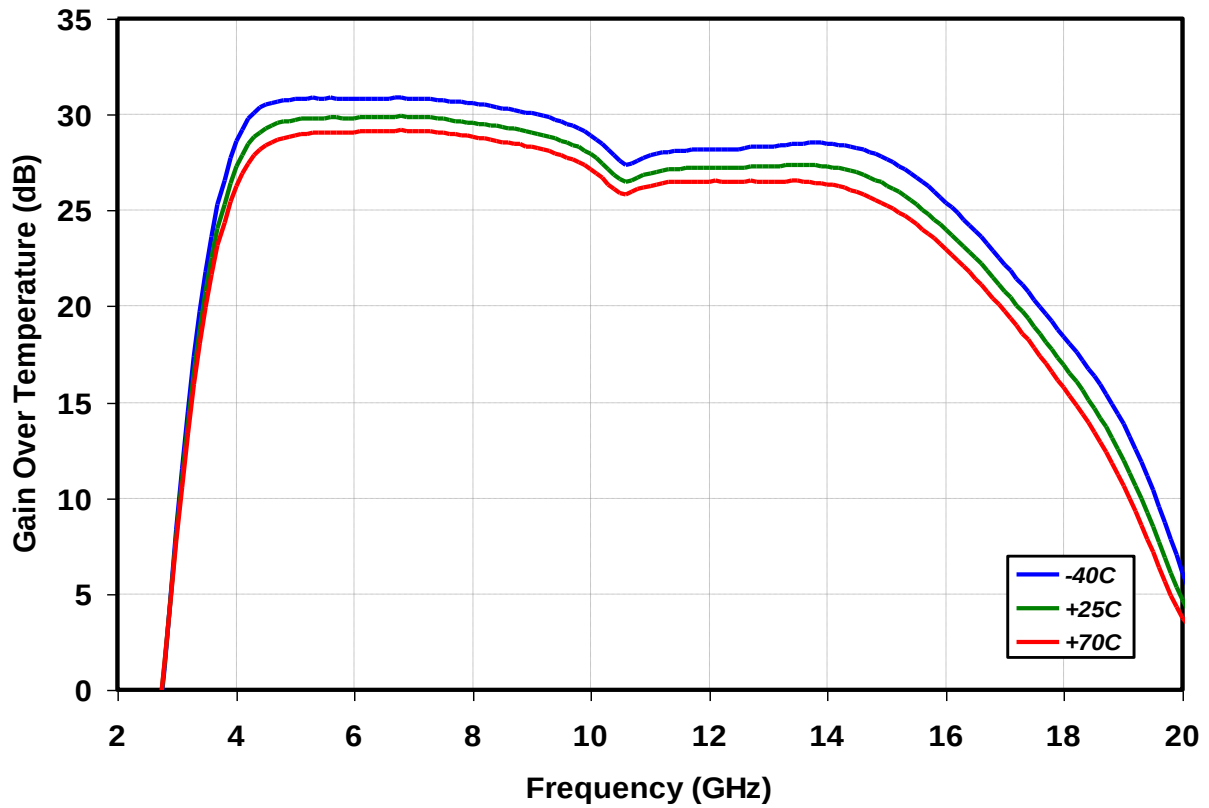
Performance Plots

Bias Conditions: Gate Bias $V_d = 5\text{ V}$, $I_d = 160\text{ mA}$, $25\text{ }^{\circ}\text{C}$



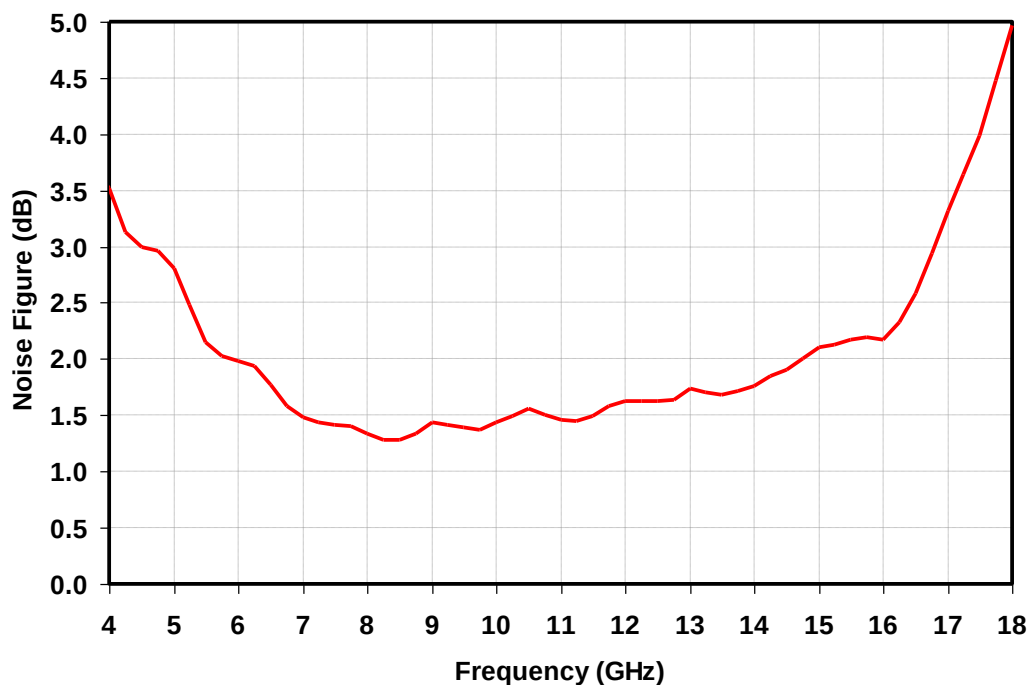
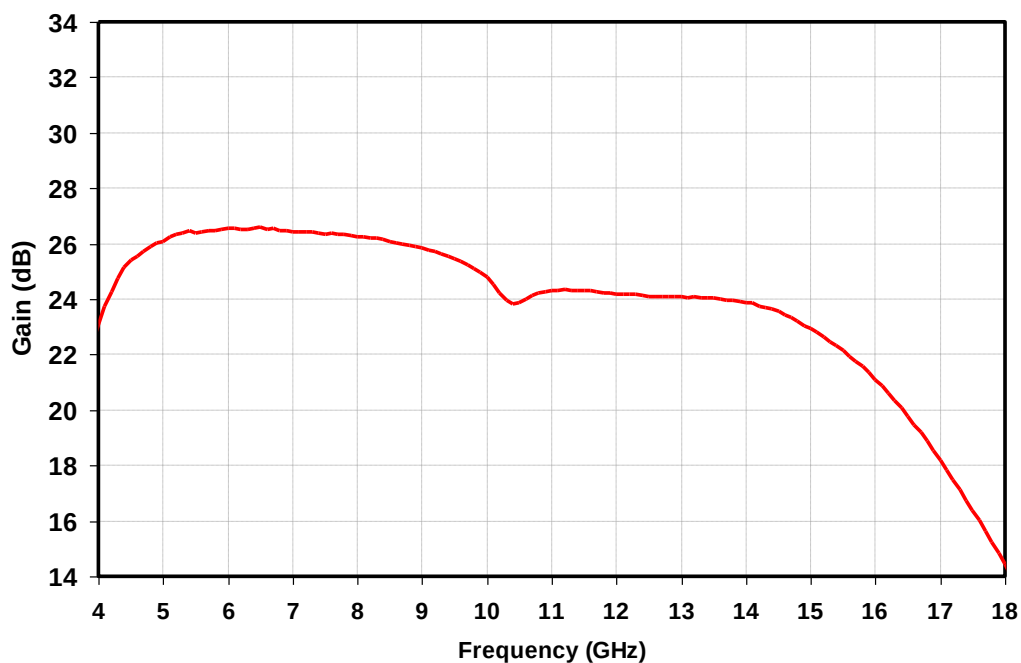
Performance Plots

Bias Conditions: Gate Bias $V_d = 5$ V, $I_d = 160$ mA, Over Temperature



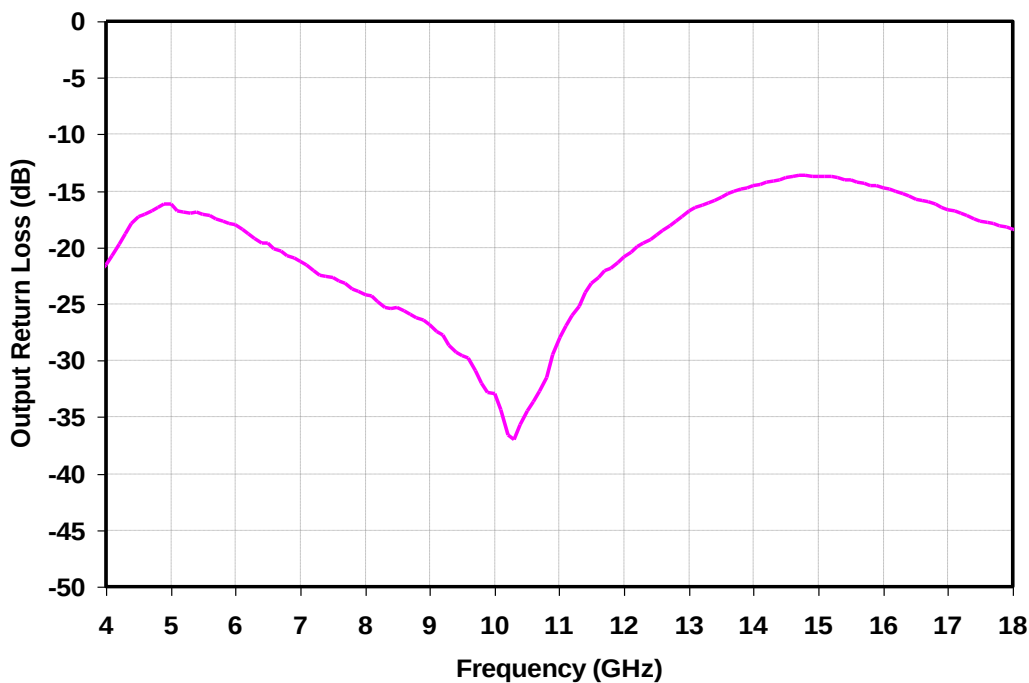
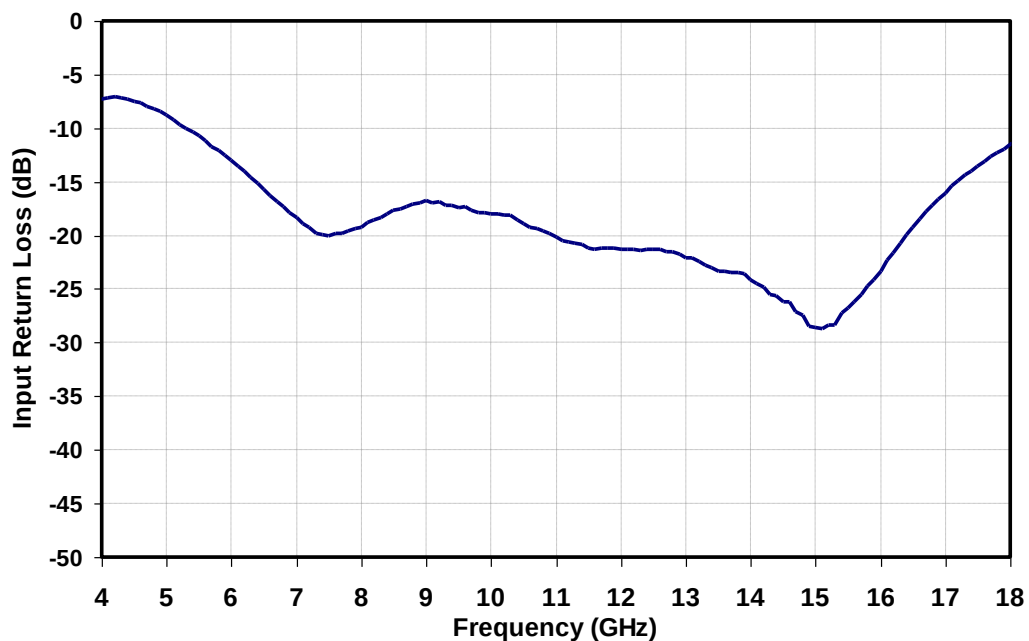
Performance Plots

Bias Conditions: Self Bias $V_d = 5\text{ V}$, $I_d = 90\text{ mA}$, $25\text{ }^{\circ}\text{C}$



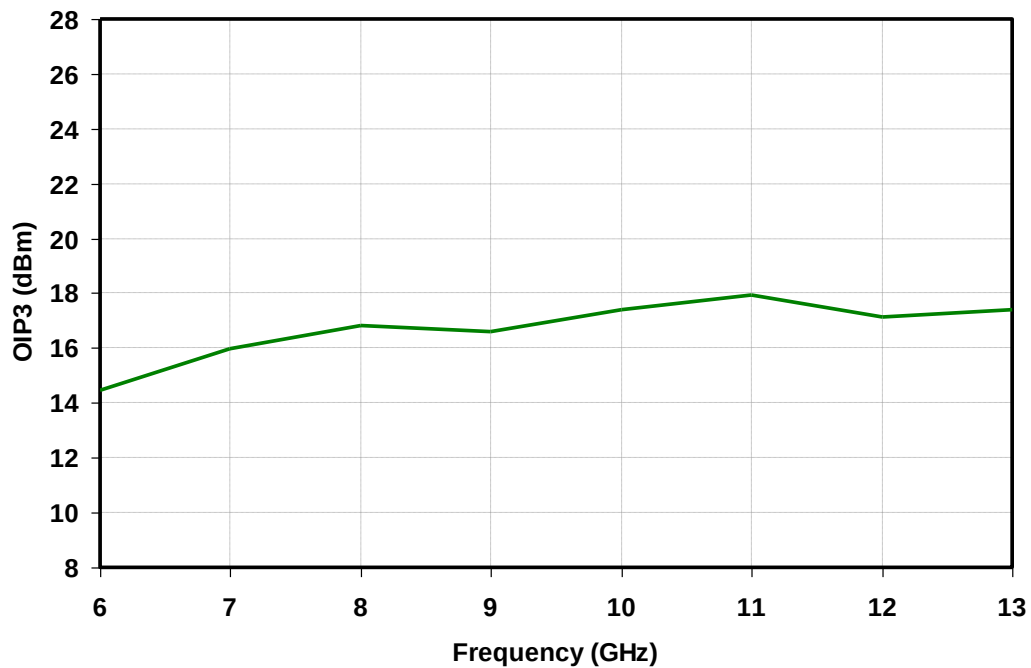
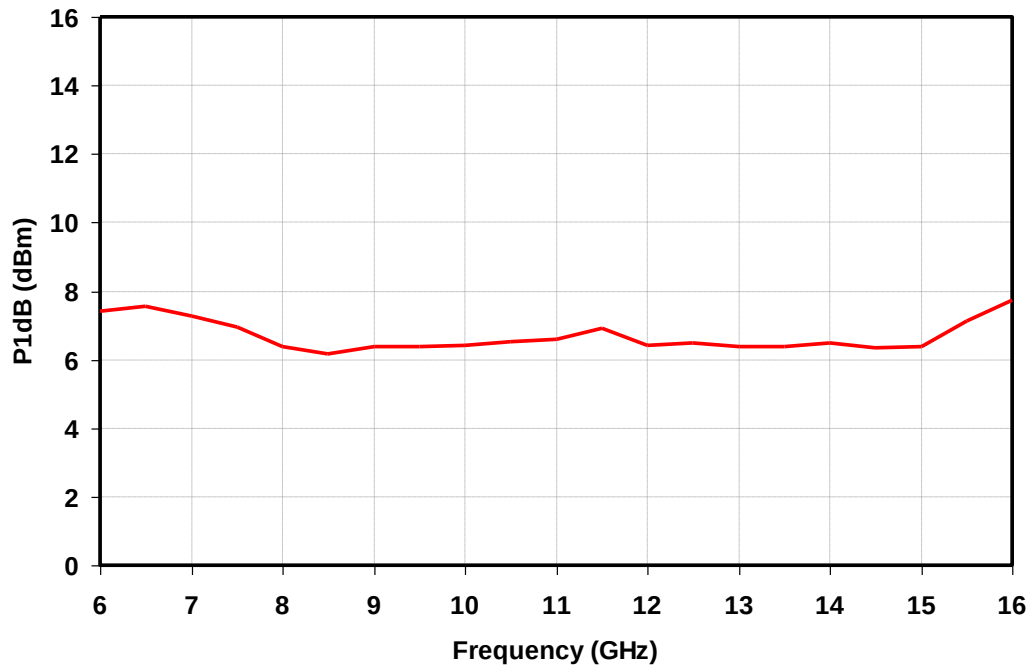
Performance Plots

Bias Conditions: Self Bias $V_d = 5$ V, $I_d = 90$ mA, 25°C



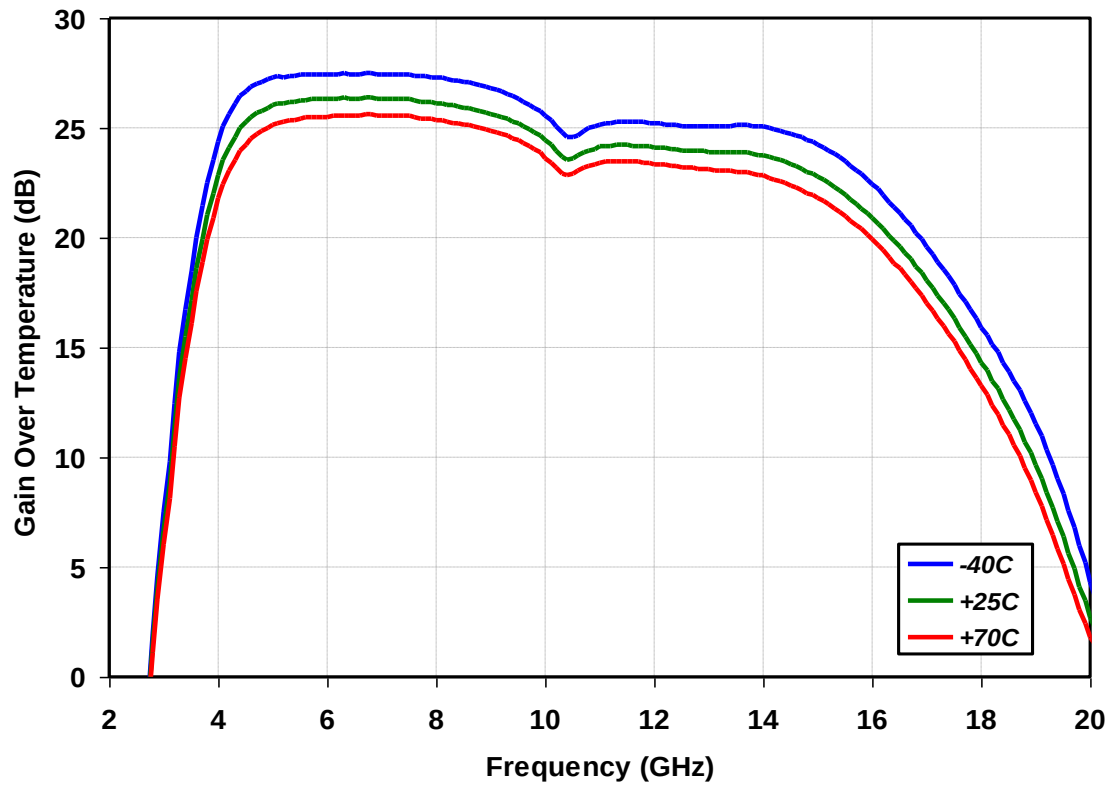
Performance Plots

Bias Conditions: Self Bias $V_d = 5\text{ V}$, $I_d = 90\text{ mA}$, $25\text{ }^{\circ}\text{C}$



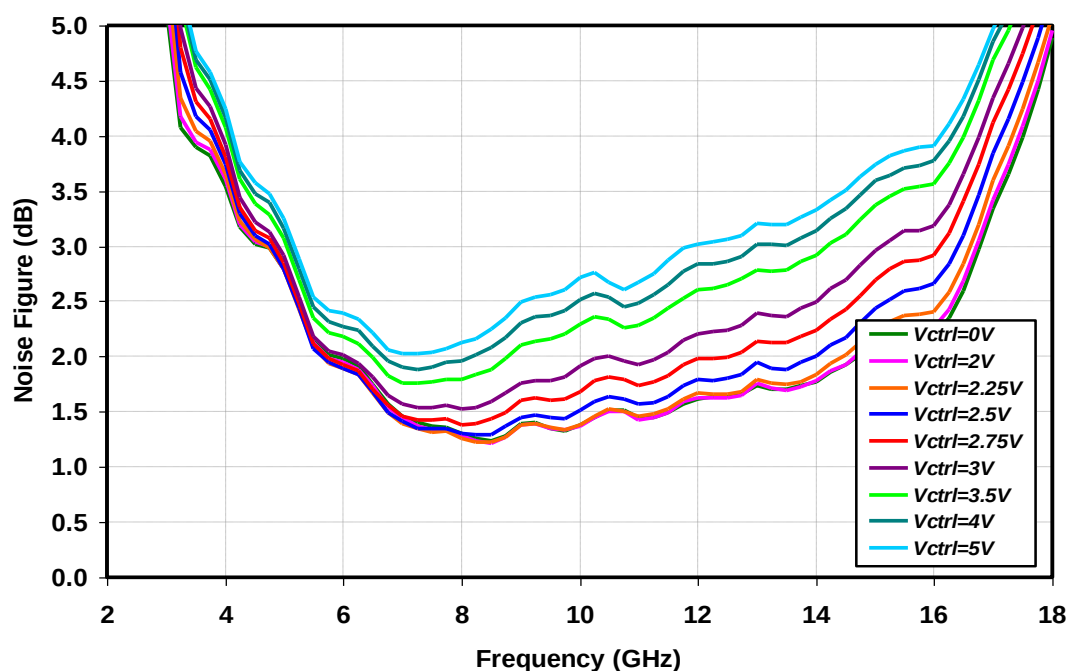
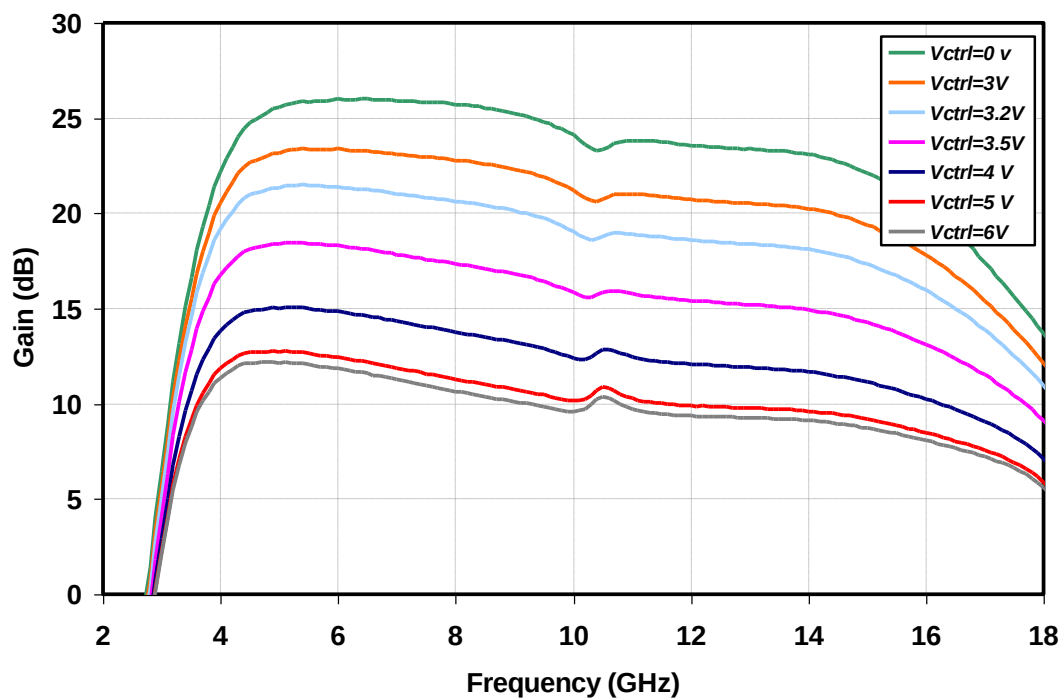
Performance Plots

Bias Conditions: Self Bias $V_d = 5\text{ V}$, $I_d = 90\text{ mA}$, Over Temperature

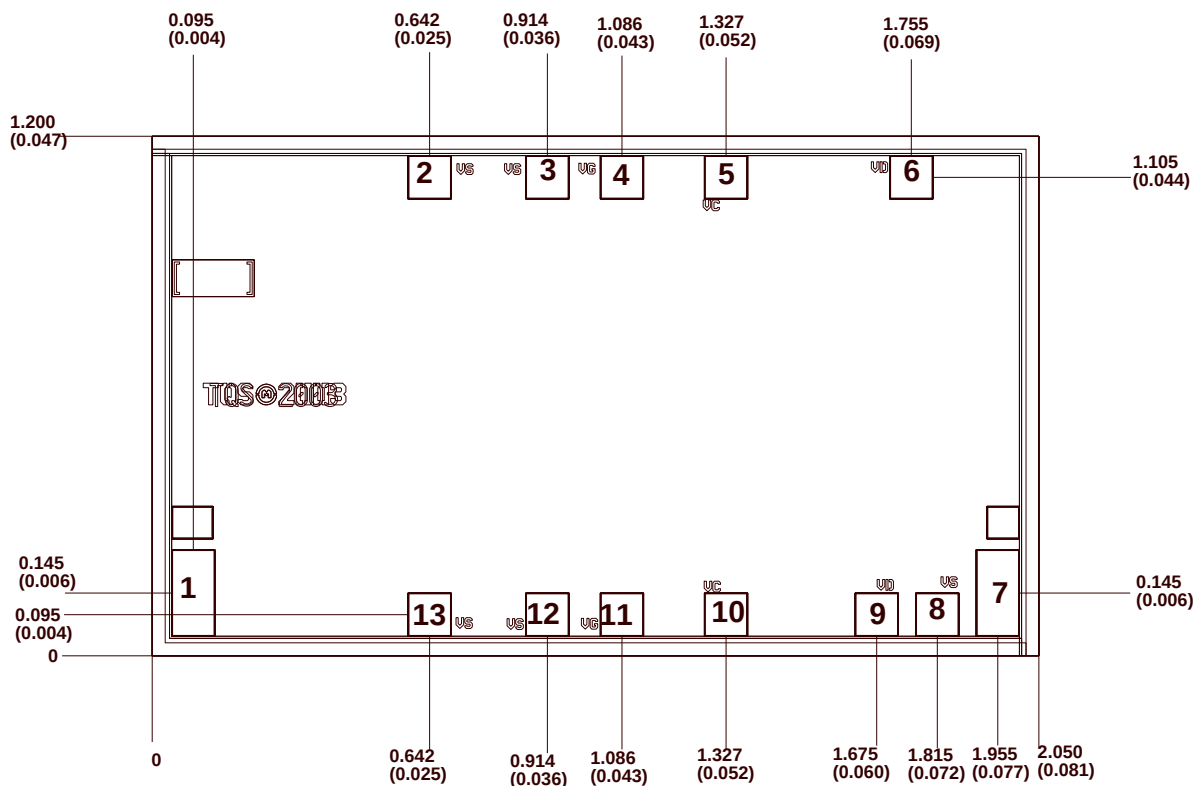


Performance Plots

Bias Conditions: Self Bias $V_d = 5\text{ V}$, $I_d = 90\text{ mA}$, $25\text{ }^{\circ}\text{C}$



Mechanical Drawing



Units: millimeters (inches)

Thickness: 0.100 (0.004)

Chip edge to bond pad dimensions are shown to center of bond pad

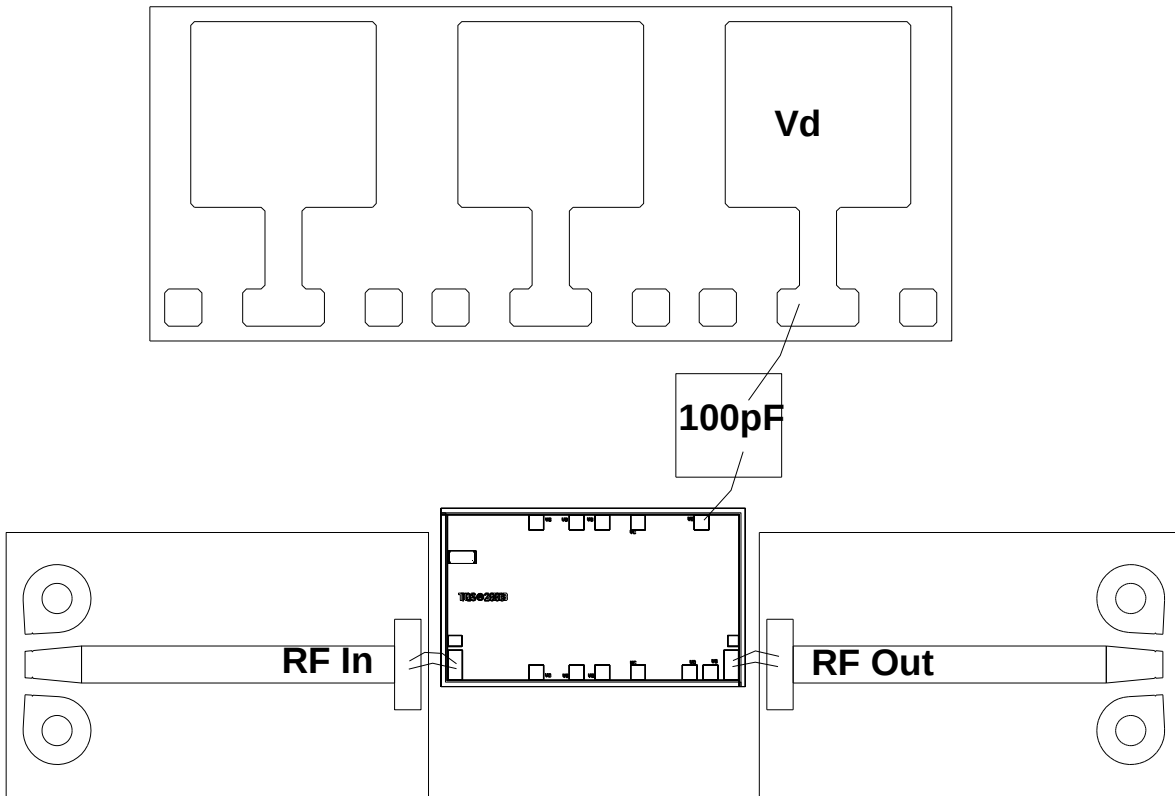
Chip size tolerance: +/- 0.051 (0.002)

GND is back side of MMIC

Bond pad #1	(RF In)	0.100 x 0.200 (0.004 x 0.008)
Bond pad #2, 3, 8, 12, 13	(Vs)	0.100 x 0.100 (0.004 x 0.004)
Bond pad #4, 11	(Vg)	0.100 x 0.100 (0.004 x 0.004)
Bond pad #5, 10	(Vctrl)	0.100 x 0.100 (0.004 x 0.004)
Bond pad #6, 9	(Vd)	0.100 x 0.100 (0.004 x 0.004)
Bond pad #7	(RF Out)	0.100 x 0.200 (0.004 x 0.008)

Recommended Chip Assembly Diagram

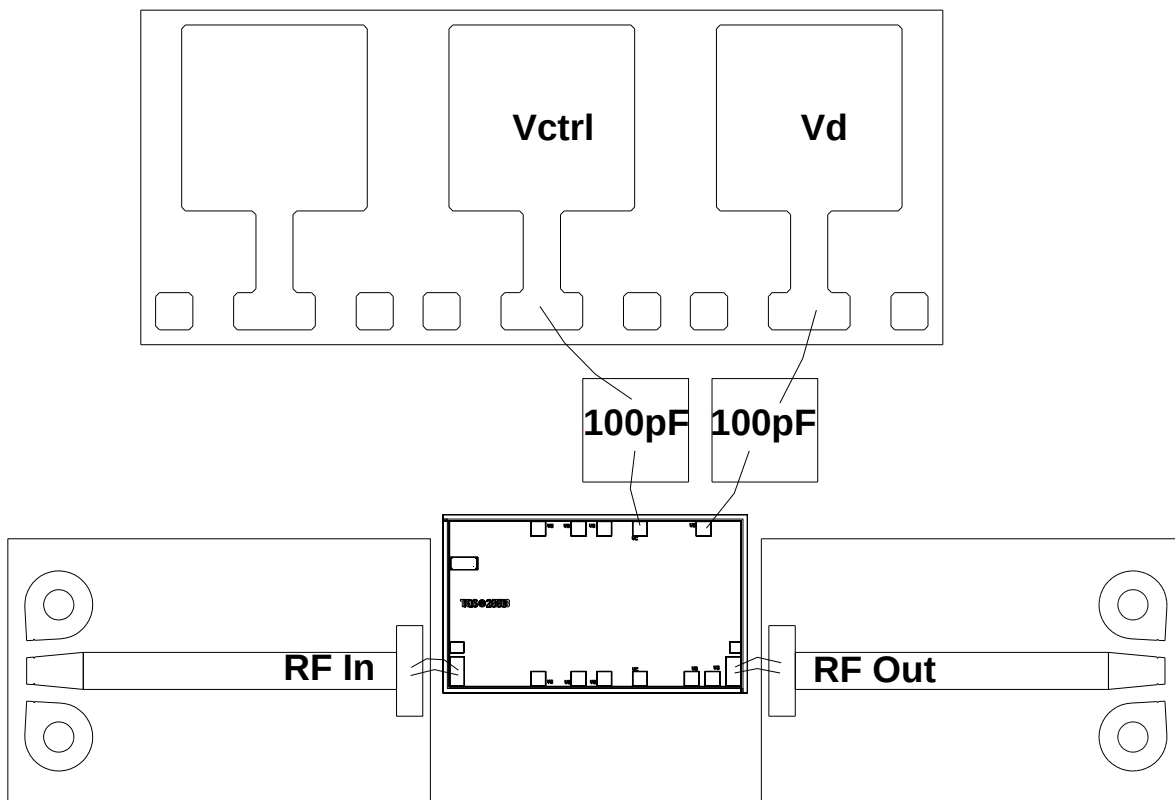
Option 1: Self Bias - No Gain Control



All DC connections may be brought in from either side of the chip (Use Pad 6 or 9)
0.01 uF external cap is recommended on drain bias: $V_d = 5\text{ V}$ ($I_d = \sim 90\text{ mA}$)

Recommended Chip Assembly Diagram

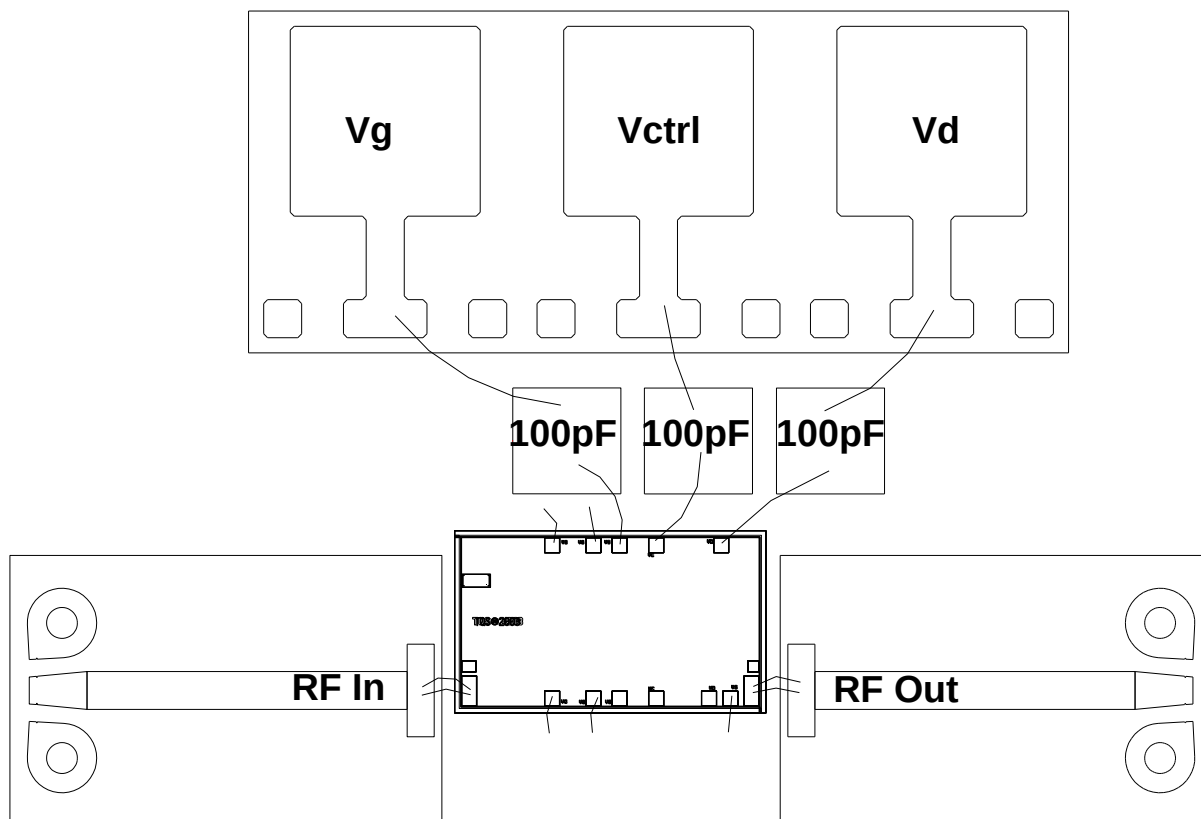
Option 2: Self Bias - with Gain Control



All DC connections may be brought in from either side of the chip (Use Pad 5 or 10, and Pad 6 or 9)
 0.01 uF external caps are recommended on drain line bias: $V_d = 5\text{ V}$ ($I_d = \sim 90\text{ mA}$)
 $V_{ctrl} = 0\text{ to }+5\text{ V}$ for gain adjustment

Recommended Chip Assembly Diagram

Option 3: Gate Bias - With Gain Control



All DC connections may be brought in from either side of the chip (Use Pad 4 or 11, Pad 5 or 10, and Pad 6 or 9).

0.01 μ F external caps are recommended on drain, gate lines.

10 ohm external series R between 100 pF cap and 0.01 μ F cap is recommended for gate line

Source connections (Pad 2, 3, 8, 12, 13) are bonded to ground.

All five bond wires are required for stability.

Bias: $V_d = 5\text{ V}$, $V_{ctrl} = 0\text{ to }+5\text{ V}$ for gain adjustment, $V_g = \text{Range, } -0.5\text{ to }0$, typically ~ -0.1 will provide $\sim 160\text{ mA}$ of I_d .

Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300 °C (30 seconds max).
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Maximum stage temperature is 200 °C.

Handling Precautions

Parameter	Rating	Standard	 Caution! ESD-Sensitive Device
ESD – Human Body Model (HBM)	TBD	ANSI/ESD/JEDEC JS-001	
ESD – Charge Device Model (CDM)	TBD	ANSI/ESD/JEDEC JS-002	

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

Important Notice

The information contained herein is believed to be reliable; however, Qorvo makes no warranties regarding the information contained herein and assumes no responsibility or liability whatsoever for the use of the information contained herein. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for Qorvo products. The information contained herein or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regard to such information itself or anything described by such information. **THIS INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.**

Without limiting the generality of the foregoing, Qorvo products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death.

Copyright 2020 © Qorvo, Inc. | Qorvo is a registered trademark of Qorvo, Inc.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Qorvo:](#)
[TGA2512](#)